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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,796	07/16/2004	Friedrich Hapke	DE02 0018 US	6921

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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/501,796	HAPKE, FRIEDRICH	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/16/2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Drawing is objected to under 37 C.F.R. 1.84(o). All features represented by boxes in the drawing must be label with a term which indicates what element the boxes represent. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-4:

The labeling of each element in the claims should be avoided because the labeling has not been labeled correctly which creates more confusing in the claims. A self-testing circuit (**5-13**) (at lines 1-2 of claim 1) refers elements 5 **through** 13 in the drawing. How can elements **6 through 8** be the first logic gates (as being recited at line 3 of claim 1)? How can elements **10 through 12** be the second logic gates (as being recited at line 7 of claim 1)? How can element **13** be a signature register (as being recited at lines 1-7 of claim 1)? How can element **5** later be a linear feedback shift register (as being recited at line 2 of claim 2)?

Claims 1 and 2:

Due to the **over** use of commas "," throughout claims 1 and 2, confusing language appears throughout the claims. In other words, most of the commas "," have been used incorrectly. Applicant should review the claims and made necessary correction.

Claim 1:

In is not clear where the preamble of the claim ends. Due to the confusing because lack of preamble, applicant is requested to reformat the claim so as to include the word "comprising: " at the end of the preamble and include an "ing" ending word for each structure after a preposition "for" (i.e. a self-testing circuit .... for testing ....).

At lines 1-3, the phrase "An integrated circuit ... with an applicant circuit ... to be tested and a self-testing circuit..., (be aware the use of commas) which is provided for testing the application circuit ... and generates pseudorandom test patterns" is confusing.

It is not clear which element tests the applicant circuit

It is also not clear which element generates the pseudorandom test patterns.

At line 3, the use of the phrase "can be" should be avoided because it is not clear whether any actually transforming function is being recited.

At line 3, due to a commas being used before and after the phrase of "which can be transformed", it is not clear what element can be transformed. It is also not clear whether that element later can be transformed by the first logic gates.

At lines 3, 6, and 7, the use of the phrase "means of" should be deleted to avoid the use of unnecessary phrase(s) in the claim.

At line 4, due to the wrong of use comma before the word "which", it is not clear whether the deterministic test vectors are being fed to the applicant circuit.

At line 5, the use of article "the" in the phrase "the output signals" lacks antecedent basis. The phrase should be replaced with "a output signals".

At lines 6-8, the phrase "a function of the test patterns are evaluated by ... a signature register, wherein, by second logic gates ..." cannot be understood.

Firstly, it is not clear what is the word "wherein" doing in the middle of the phrase. Secondly, it is not clear whether the signature register or the second logic gates evaluate(s) the function of the test patterns.

At line 7, the term "said gates" is indefinite because it is not clear whether the term should refer to the first logic gates or the second logic gates.

At line 8, it is not clear whether or not the phrase "those bits of the output signals" referring to all bits of the output signals.

At lines 8-9, the term "the circuit structure" lacks antecedent basis. It is not clear what the structure the circuit referring to.

At line 9, in what condition is being consider as "undefined states"? What is being in the undefined states? The "those bits of output signals" (at line 8)?

At line 9, what is being block during testing?

Claim 2:

At line 2, a comma "," should be delete after the word "linear".

At lines 2-4, due to the over use of commas "," , it is not clear whether the self-testing circuit or a linear feedback shift register generates pseudorandom test patterns. It is also not clear whether the self-testing circuit, the linear feedback shift register, or the first logic gates transform(s) the pseudorandom test patterns into predeterminable deterministic test patterns.

At line 3, it is not clear whether or not the term "pseudorandom test patterns" refers to the previously recited pseudorandom test patterns (as being claimed at line 3 of claim 1). If it is, the term "pseudorandom test pattern" should be replaced with –said pseudorandom test pattern".

At lines 3-4, it is not clear whether or not the phrase "predeterminable deterministic test patterns" refers to the previously recited deterministic test vectors (as being claimed at line 4 of claim 1). If it is, then the term "predeterminable deterministic test patterns" should be replaced with –said deterministic test vector--. In other words, consistency of a term should be used throughout all claims.

At lines 3 and 4, a comma "," should be delete.

At line 4, the use of the phrase "means of" should be deleted to avoid the use of unnecessary phrase(s) in the claim.

Claim 3:

At line 2, it is not clear whether or not the phrase "those bits of the output signals" referring to all bits of the output signals.

At line 3, it is not clear actually which elements of the phrase "those circuit elements" referring to.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/506,234. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application substantially teaches the claimed invention. The copending application '234 does not explicitly teach the feature of generating pseudorandom test patterns. However, the copending application '234 teaches the feature of generating desired test patterns (at line 3 of claim 1). It would have been obvious to one skilled in the art at the time the invention

was made to realize that the desired test patterns (of the copending application '234) would have been pseudorandom test patterns. One having ordinary skill in the art would be motivated to realize so because the copending application '234 suggests the pseudo-random sequence in the test patterns (at line 8 of claim 1).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhawmik (6,370,664).

Claims 1 & 4:

Bhawmik discloses the invention substantially as claimed. Bhawmik teaches (figures 1 & 2) that a BIST structure includes a test pattern generator (10) for generating random patterns, via a scan chain (21) comprising flip-flops (F1-Fn) to pseudo-inputs (22) of combinational elements (20). Data from the primary outputs (30) of the IC and via the scan chain (21), are output to a response analyzer (35) which can be a multiple input signature register (MISR). The response analyzer (35) serves to compact output data generated by the combination elements (20) with the captured data output from the

scan chain (21) and compares the two to yield a deterministic signature (figures 1 & 2, column 2 lines 23-56; column 3 line 54-column 4 line 44).

Bhawmik does not explicitly teach signals externally fed to the first and the second logic gates. Bhawmik does teach the flip-flops (F1-Fn) in the scan chain (column 3 lines 56-65). It would have been obvious to one skilled in the art at the time the invention was made to realize a clock (external to Bhawmik's BIST Structure) would have been encompassed in Bhawmik's invention for generating clock signals to the flip-flops (F1-Fn). One having ordinary skill in the art would be motivated to realize so because the use of a clock signal to clock a flip-flop is well-known in the art.

Claim 3:

Bhawmik further teaches (figure 2) that the flip-flops (F4-Fn) are being partitioned as a second stage (S) in the scan chain (21). Such partition S2 is still being part of the shift register that can provide storage behavior (figure 2, column 4 lines 3-5,column 3 lines 56-58).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhawmik as applied to claim 1 above, and further in view of Kim (5,574,733).

Claim 2:

Bhawmik does not teach the LFSR. Kim, however, teaches that a scan chain (391) comprises a LFSR (340) (figure 3). It would have been obvious to one skilled in the art at the time the invention was made to realize Bhawmik's scan chain (21) would

have been comprised of a LFSR (as suggested by Kim). One having ordinary skill in the art would be motivated to realize so because Bhawmik teaches the scan chain (21) could comprises as many flip-flops as desired and can be partitioned into as many partitions as desired (figures 2 & 3 column 3 lines 58-62, column 4 lines 45-52).

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2133

September 10, 2005